

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an amorphous insulative layer having a dielectric constant greater than five, the insulative layer formed between the conductive layer and the surface region;

a self-aligned source region formed along the surface region and having a second conductivity type; and

a self-aligned drain region formed along the surface region and having a second conductivity type, said gate structure, source region and drain region configured to form an operable self-aligned field effect transistor, said source region and said drain region directly self-aligned with the gate structure.

7. The device of claim 6 wherein the insulative layer comprises  $Ta_2O_5$ .

8. The device of claim 6 further including a layer of  $SiO_2$  disposed between the insulative layer and the surface region.

9. (Amended) A semiconductor device comprising:

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an amorphous insulative layer having a dielectric constant greater than 5, the insulative layer formed between the conductive layer and the surface region; and

a self-aligned source region and a self-aligned drain region, each formed in the surface region, directly self-aligned with the gate structure and on a different side of the gate structure,

said gate structure, source region and drain region configured to form a self-aligned field effect transistor characterized by a gate leakage current less than  $0.1 \text{ amp per cm}^{-2}$  during operation.

10. The device of claim 9 wherein the field effect transistor is characterized by a gate leakage current less than 10 milliamps per  $\text{cm}^{-2}$  during operation.

11. The device of claim 9 wherein the field effect transistor is characterized by a gate leakage current less than one milliamp per  $\text{cm}^{-2}$  during operation.